

Fast Data Acquisition, Signal Processing and Its Integration Within Instrument Control

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ESI - 17 May 2011

Outline

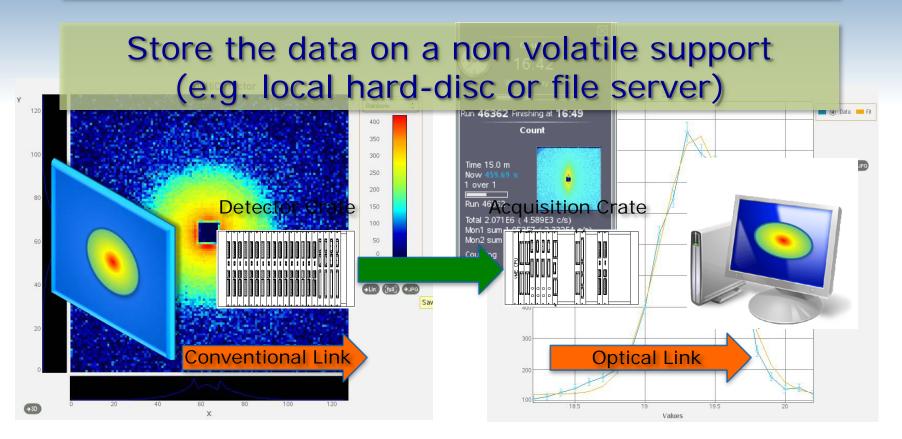


- Basics of signal detection
- Analog approach
- Digital approach
- Acquisition modes
- Integration within the sequencer



Acquisition - The Goal

Obtain a numerical or graphical representation of the events arriving at the detector





Acquisition - Requirements

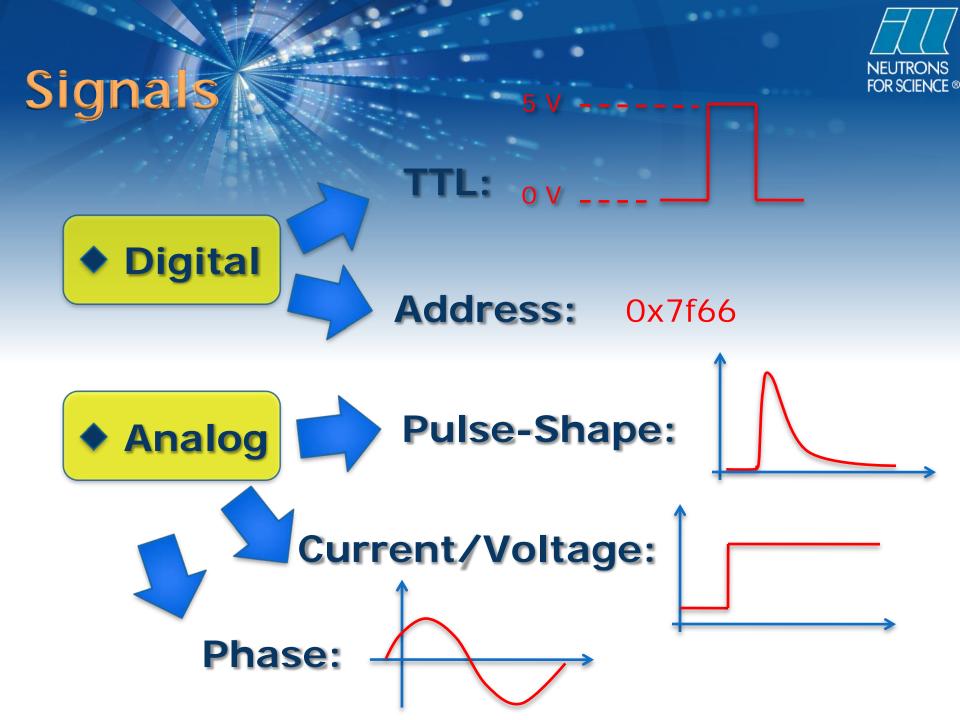






High Data Throughput

Synchronization With Other Operations





Signals Acquisition



Scalers Digital I/O



Sampling ADC

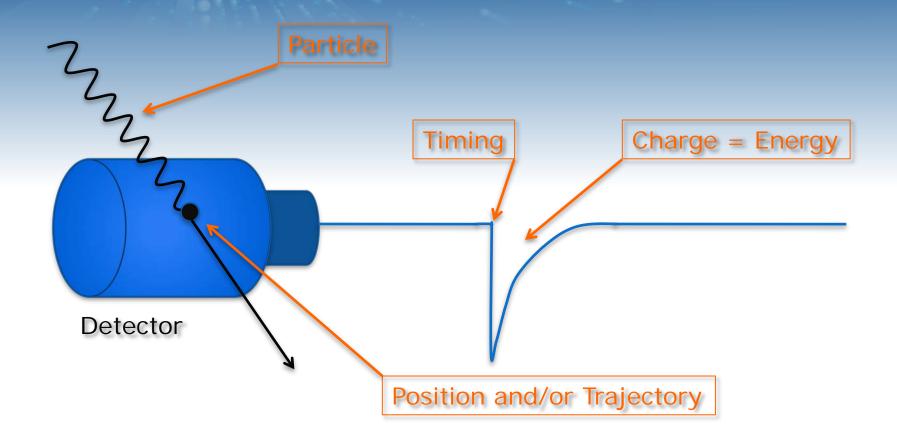
Peak-Sensing ADC

Digitizers

Multi-Channels Analyzers



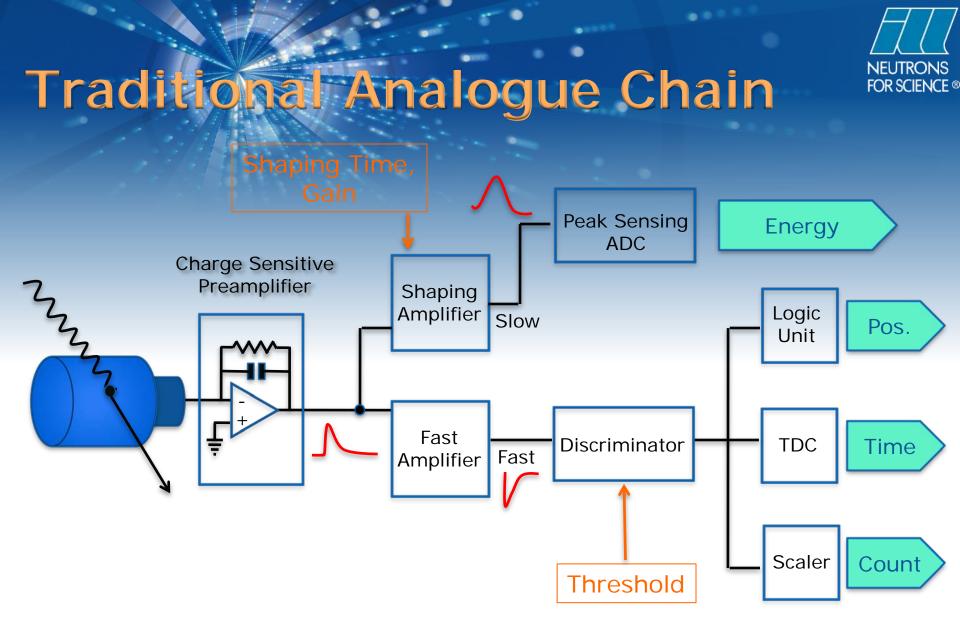
The Relevant Quantities



Outline



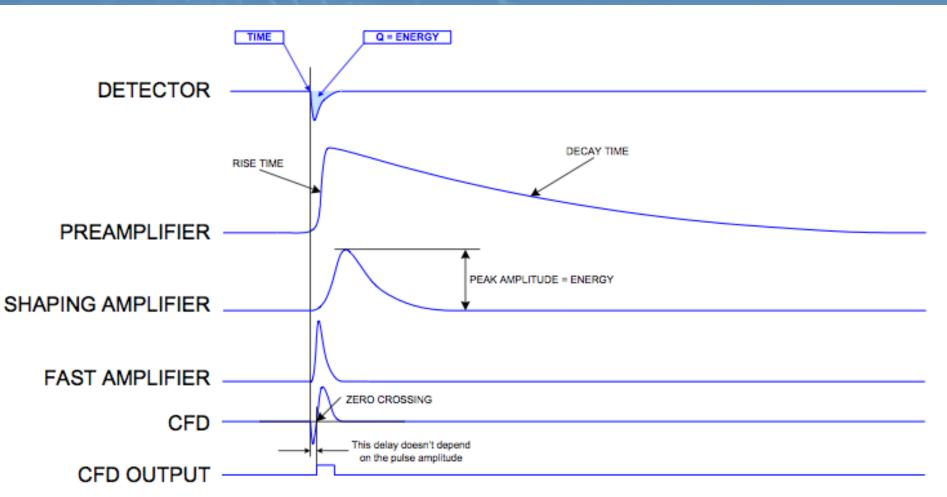
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Analog Signals



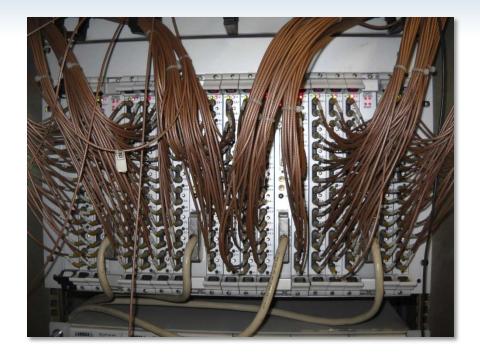


Analog Acquisition



One channel energy-time

256 x 128 pixels



Outline

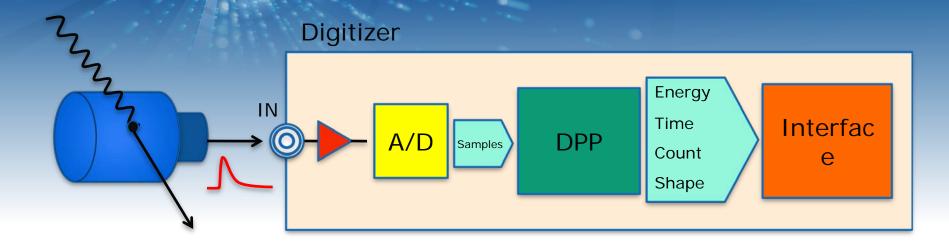


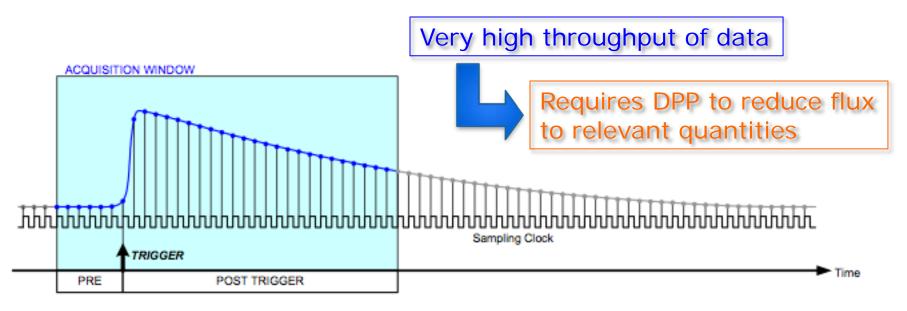
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Digital Chain

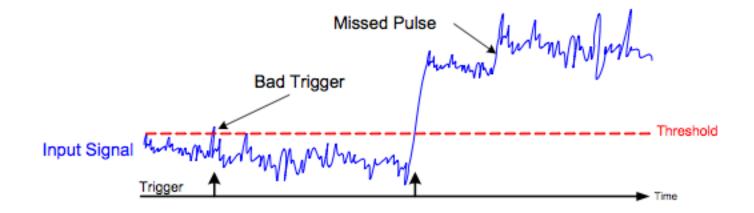






Trigger and Timing Filter

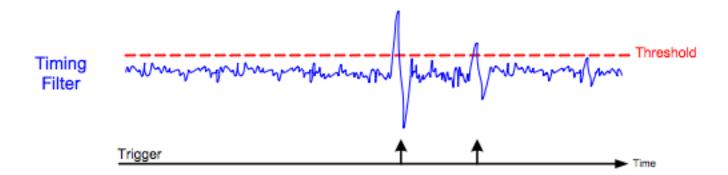
- A trigger is generated as soon as the signal cross the threshold
 - Noise and base-line variation can generate bad triggers
 - Loss of pulses due to pile-up





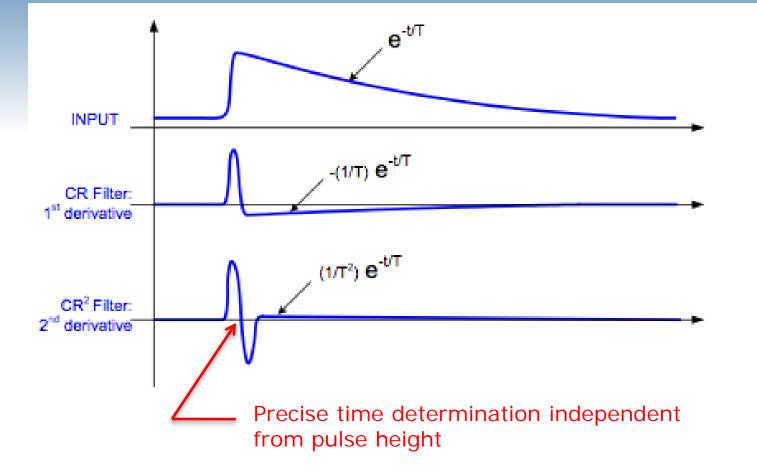
Trigger and Timing Filter

- Digital filters are able to reject the noise and restore the base-line
 - RC filter (mean) for high frequency noise
 - CR^N filter (derivative) for low frequency noise
 - Transform signal in bipolar for better timing (zero crossing)



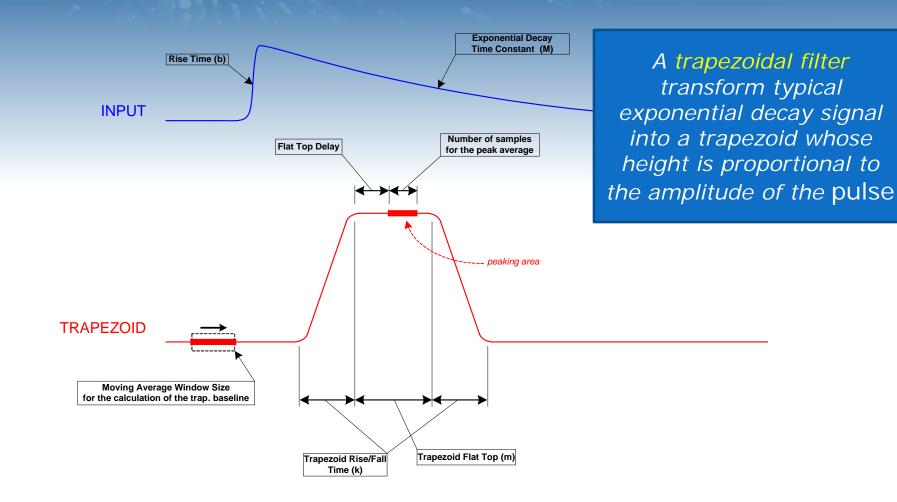


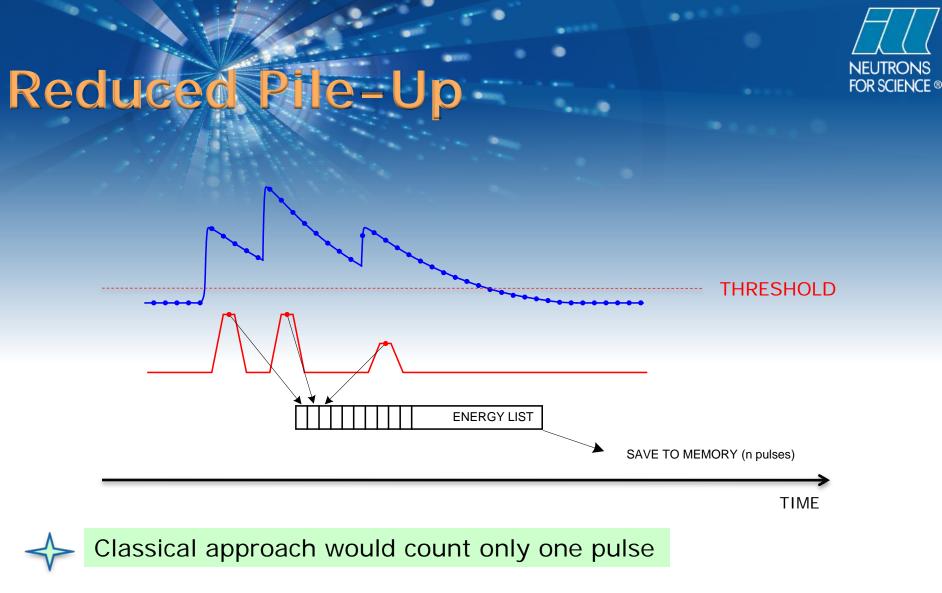






Pulse Height Analysis

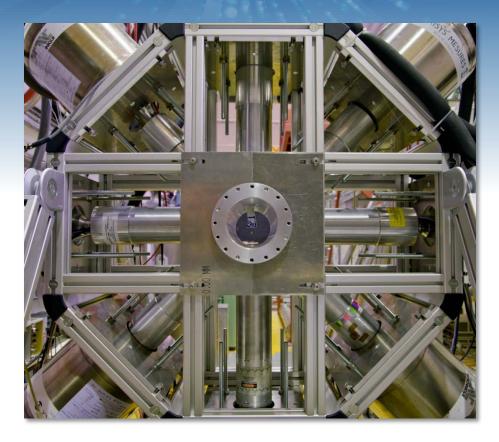




 Digital approach separates pulses as far as trapezoids do not overlap



Digital Acquisition





Detection System

Acquisition System



A/D Comparison

ADVANTAGES

- × One single board can do energy, timing and pulse shape analysis.
- × Low cost per channel and reliability.
- × Low dead-time in the acquisition.
- Synchronization and correlation among several channels (coincidence).
- × All in FPGA, flexibility in tuning and calibration.

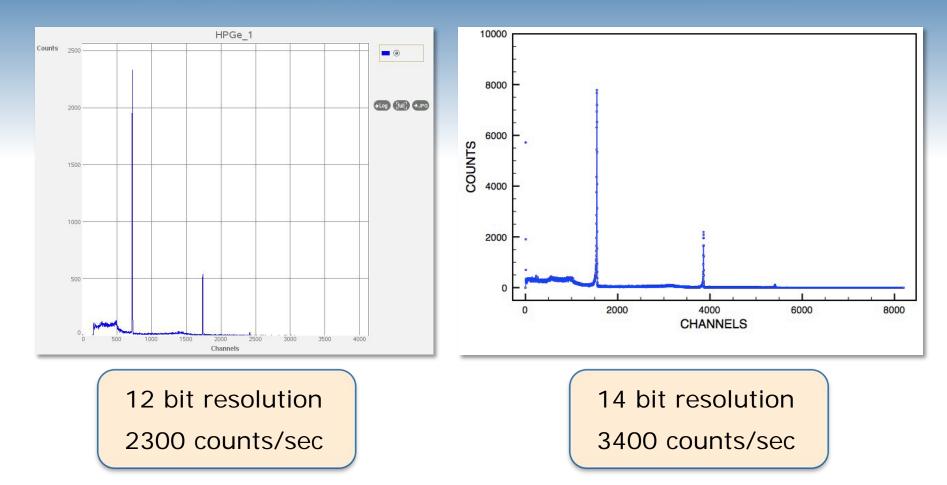
DISADVANTAGES

- Setting up the system requires time and a knowledge of the relevant parameters.
- Loss of resolution with fast signals. We are limited by the bit number and sampling rate.



A/D Comparison

NA SOURCE (511 + 1274 KEV GAMMAS)



Outline

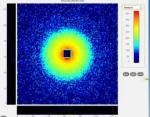


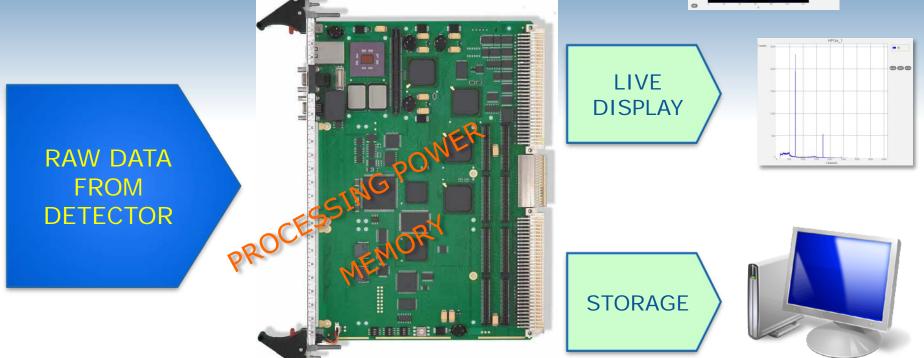
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The Acquisition Card



PowerPC VME based cards using PMC or MFCC modules for multi-detector acquisition

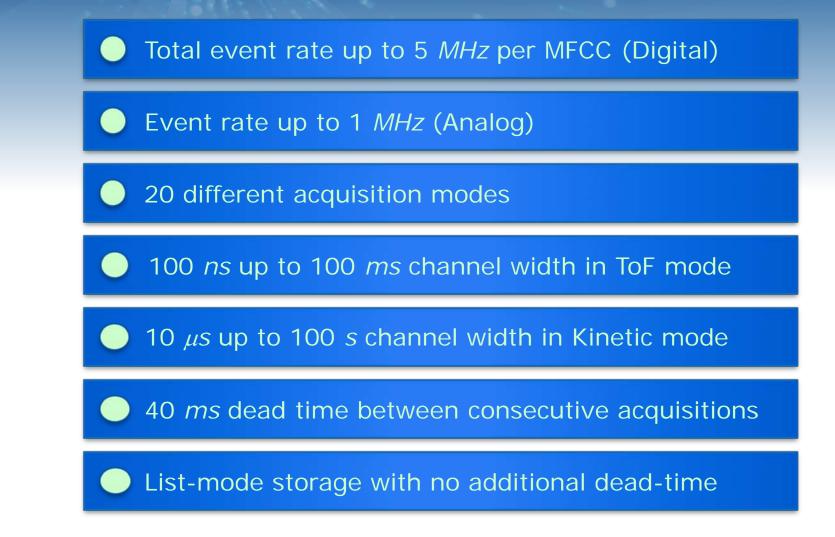




Its main role is to rearrange the data according to the user's need before the final storage

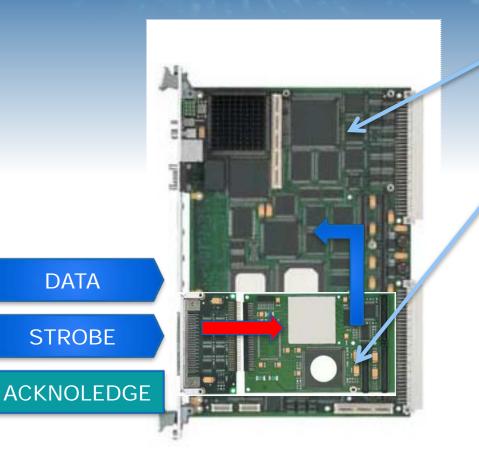


Requirements



The RIO2 Family





- Motherboard: RIO2 8062
- Clock: 400 MHz
- Memory: 32 Mb
- PMC: GPIO 8405

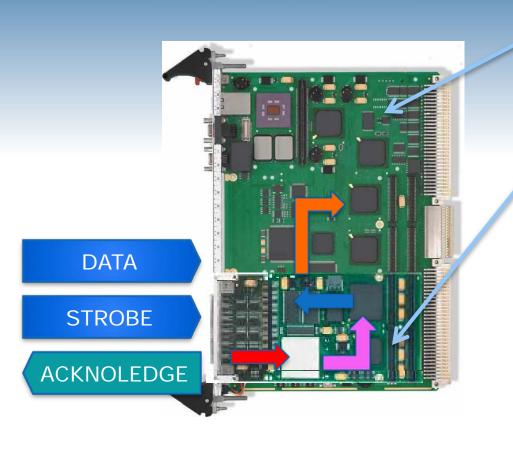
Data from detector



Readout from FIFO (PCI) and storage in RAM

The RIO3 Family





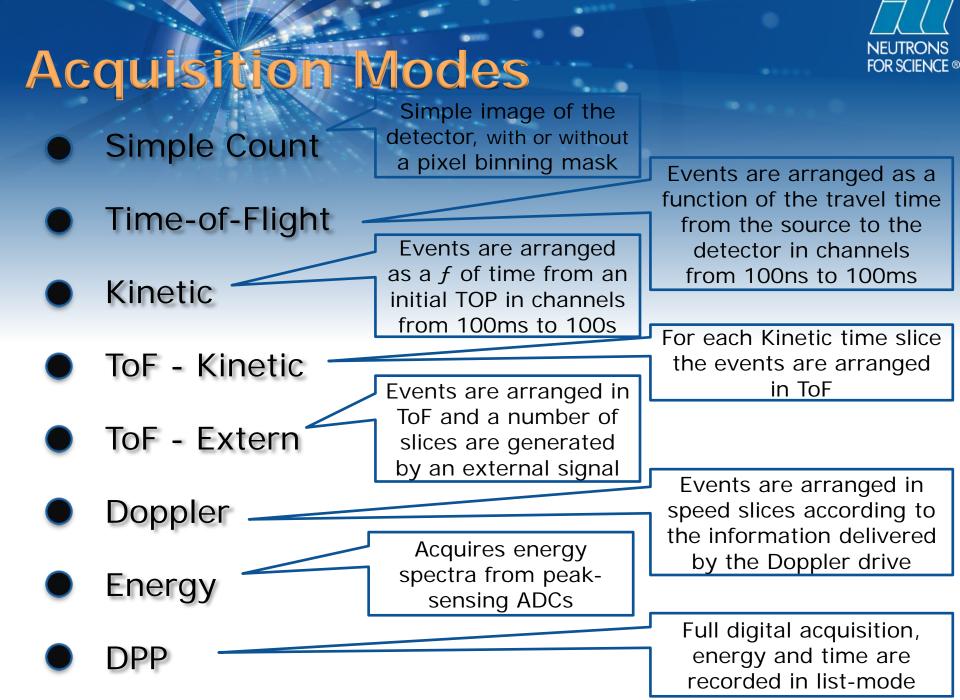
- Motherboard: RIO3 8064
- Clock: 400 MHz
- Memory: 256 Mb
- PMC: MFCC 8443 (128 Mb)

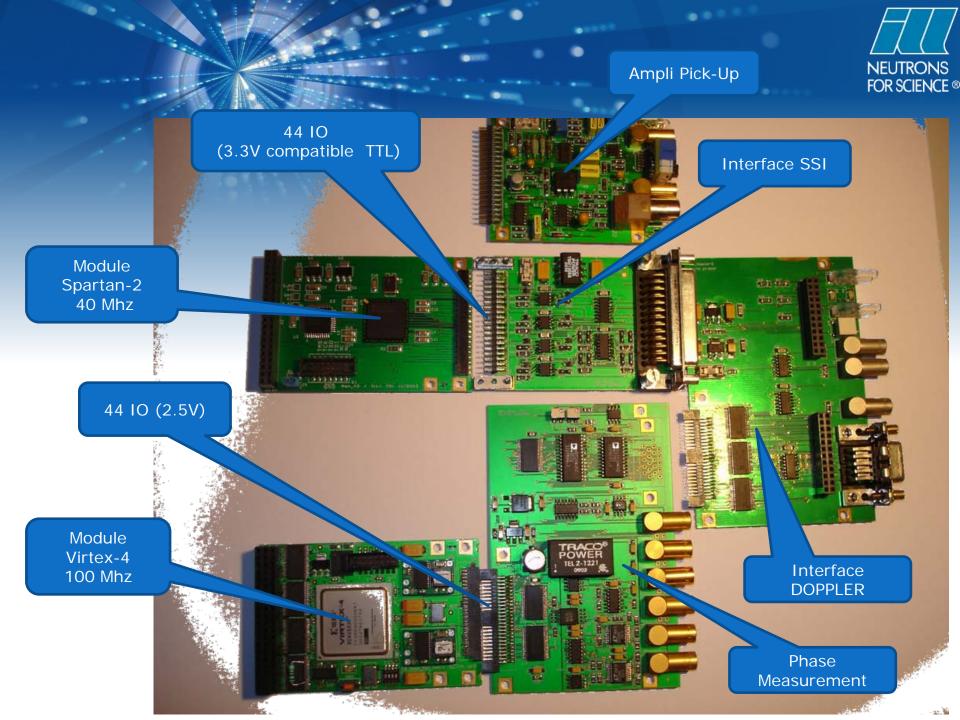






DMA MFCC -> RIO3





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Digitizer Tuning

| Nuclear Settings RASDPP_II RASDPP_II RASDPP_II RASDPP_II Pelage rankers RASDPP_II RASDPP_II Pelage rankers RASDPP_II RASDPP_II Pelage rankers RASDPP_II RASDPP_III Pelage rankers RASDPP_III RASDPP_III Redamestic Instance Retainer RASPP rankers RASPP rankers RASPP rankers RASPP rankers RASPP rankers RASPP rankers RASPP rankers RASPP rankers RASPP rankers | | | mad | | | | _ 🗆 X | | | |
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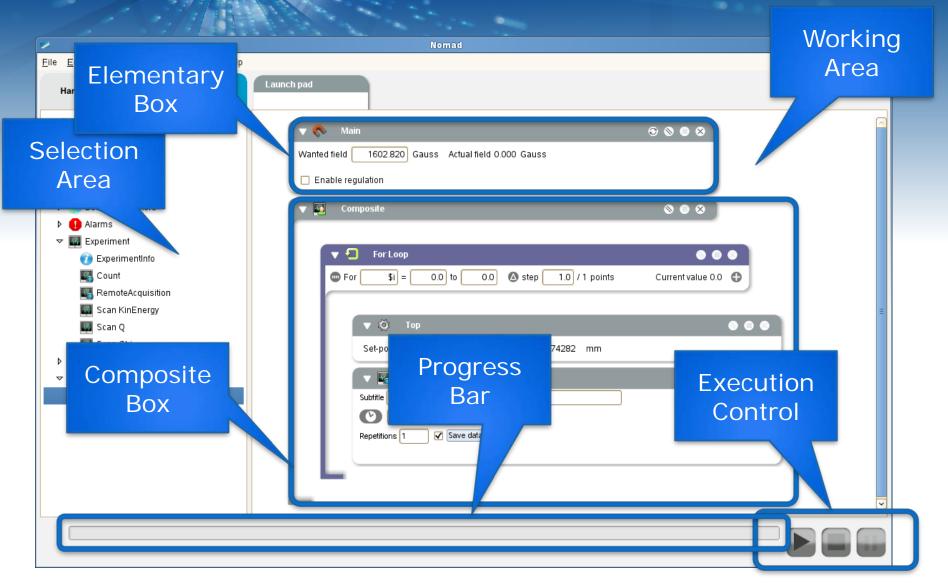
Doppler Tuning

| 1 | Nomad | _ = × |
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| <u>File Edit View Hardware Command Help</u> | | |
| | Nomad Voppler Set Doppler by Speed ♀ 0.00 m/s Amplitude 75.0 mm 0.00 mm Speed profile Sine ♀ T 1.00 µs T2 5600.00 µs | ► More options Summary Actual wavelength £ 27 Å Actual ΔE 0.00 µeV Actual ΔE 0.00 µs T2 0.00 µs Status: ● Ready |
| | | |

A Graphical Control



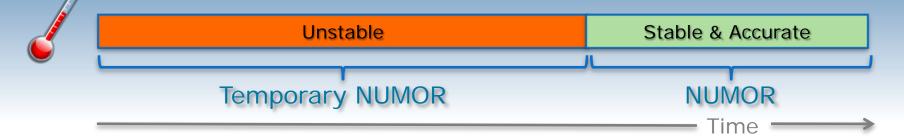
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Software – Hardware Integration

Temperature Watchdog



O Double Buffering

- Reduce the dead-time between successive acquisitions
- Allow high data throughput from acquisition electronics to the final storage
- Necessary for list-mode (up to 1Tb per day)



Summary



- Examples of ILL's acquisitions
- ٠
- Implementation of acquisition functionalities within the control software

Thanks for your attention